VIPerXX0 FAMILY DEVICES IN STANDBY SMPS

by A. Bailly

1. Scope

This document presents the results obtained from a standby off line power supply designed with a VIPer100. The first part describes the standard design for an output power up to 3.5W, and the second makes some modifications to address other operating conditions : Output power from 0W to 30W, output short circuit and lower switching frequency.

2. Schematics

The standby power supply breadboard is based on the standard 12V wide range 50W flyback demoboard, by making some component adjustments. The complete schematics of this standby power supply is shown in figure 1.

The following are the modifications from the standard demoboard:

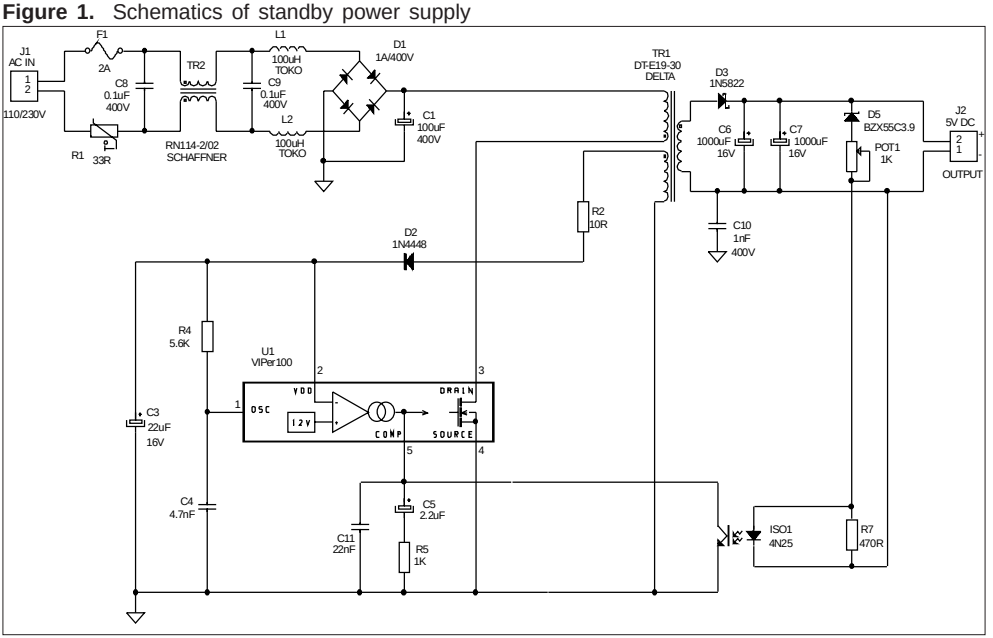
1. The clamper on the drain of the VIPer100 has been taken out. It is no longer needed with such a low output power. It can be seen that in nominal full load condition, the peak drain voltage doesn't exceed the maximum rated one. It can be overpassed at start up, where the device may absorb some avalanche energy. This doesn't prevent the device from running correctly, because of its' avalanche ruggedness.

2. The transformer is suited to deliver 5V / 750mA output power.

3. The secondary rectifying diode is a schottky in order to improve the overall efficiency with such a low output voltage. Also, the regulating zener diode D5 has been lowered to 3.9V.

4. The output LED has been taken out.

Figure 1. Schematics of standby power supply



5. A resistor R7 has been added across the diode of the optocoupler to increase the biasing current of D5. This improves the dynamic performance of the power supply.

6. The compensation network has been adapted to provide soft start, thanks to the high value of C5. C11 has been increased to 22nF to filter the noise on the compensation pin, because the VIPer100 is working with very low levels on the compensation pin to control an output power of a few Watts. This capacitor should be lowered or omitted with a VIPer50 or VIPer20.

7. The switching frequency has been set at 77kHz through the value of R4.

3.0. Measurements

Unless otherwise noted, all measurements have been made with a high voltage DC source, ranging from 100V to 400V. This corresponds to an AC input voltage ranging from 85VAC to 280VAC.

3.1. Efficiency

Figure 2 gives the efficiency measured for 4 values of input voltage and in the whole output current range.

Figure 2. Efficiency

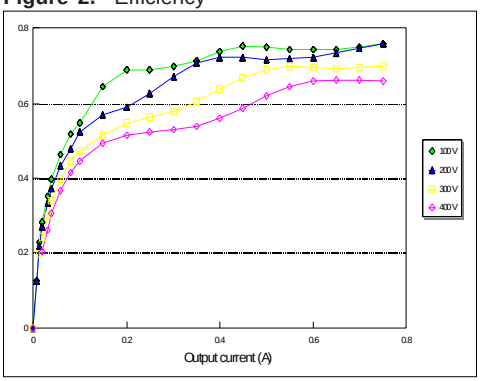


Table 1. Numerical Values

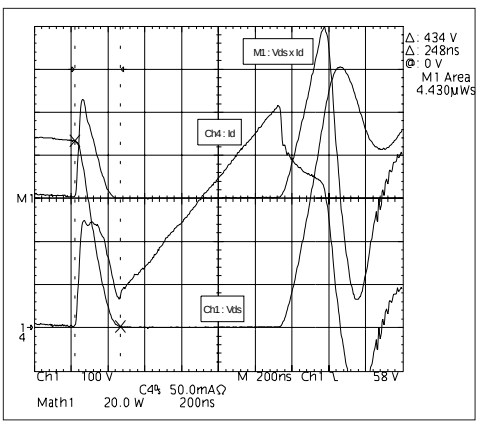
Input Voltage	Efficiency at 300mA	Efficiency at 750mA
100V	70%	76%
200V	67%	76%
300V	58%	70%
400V	53%	66%

It can be seen from the curves that the switching losses are preponderant versus conduction losses (waves). These losses have been estimated from the following scope waveforms at 400V and full load :

Turn on losses :

$$P_{ON} = 4.43\mu J \bullet 77kHz = 0.34W$$

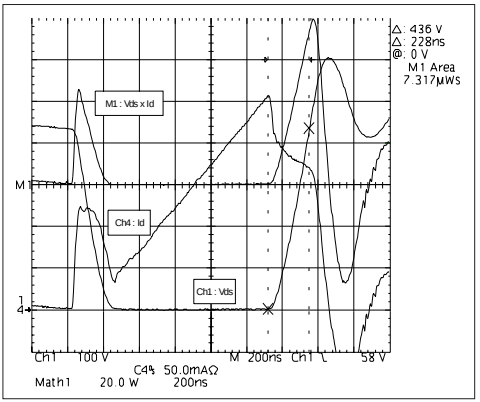
Figure 3. Turn on losses



Turn off losses :

P_{OFF} = 7.32µJ • 77kHz = 0.56W

Figure 4. Turn off losses



Note that the right cursor has been set at the same value as the turn on voltage. This assumes that nothing is dissipated at turn off, because the cross over time is only due to capacitor charging (The one of the device itself) and the internal turn off of the power mosfet is sufficiently fast. The corresponding energy of this capacitor is dissipated at turn on, and this explains that only the part of voltage which is discharged at turn on is taken into account at turn off.

The conduction losses can be estimated as follows:

$$P_{CD} = \frac{t_{on}}{t_{sw}} \bullet R_{dson} \bullet \frac{Ip^2}{3} = 0.004W$$

Table 2. VIPer100 Power Dissipation

Parameter	Value
P_{on}	0.34W
P_{off}	0.56W
P_{cd}	0.004W
P_{bias}	0.14W
P_{dd}	0.14W
P_{tot}	1.184W

Other VIPer100 dissipation includes the one of the start up biasing resistor and of the signal part. They are all reported in table 2.

The measured case temperature was 89°C for an ambient at 23°C. This corresponds to a dissipated power of about 1.1W with a thermal resistance of 60 °C/W (Free air, no heatsink) well in accordance with the above losses.

Note that the switching losses are not well balanced between the conduction losses and switching losses (0.56W vs 0.004W). This is due to the size of the VIPer100 which is not suited for such a low output power. VIPer20 should offer lower switching losses by still maintaining conduction losses at a reasonable level. This results in a better overall efficiency.

From the measurement of the overall efficiency, the total losses are about 1.9W. It can be spread as demonstrated in table 3.

Table 3. Total Losses

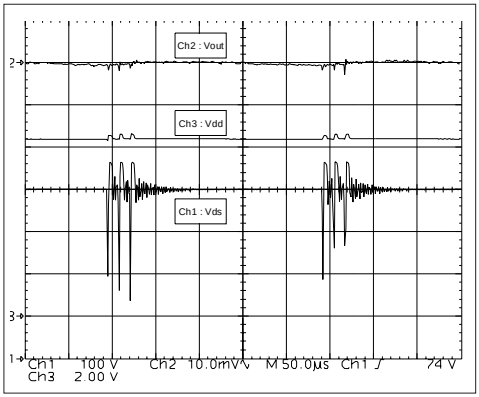
Device	Dissipated Power
VIPer100	1.18W
1N5822	0.3W
Transformer (estimated)	0.4W
P_{tot}	1.88W

By optimizing the choice of the device (VIPer20 instead of VIPer100), 0.3W can be saved, giving a total loss of 1.6W and an overall efficiency of 69% (Vin = 400V, full load). Also, the case temperature increase versus ambient temperature will be about 50°C, allowing a normal operation without heatsink for ambient temperature up to 70°C.

3.2. Burst modes

When the output current is too low, the minimum duty cycle fixed by the internal blanking time of the device is too high to control the output voltage. In such a case, the burst mode operation takes place automatically, thanks to the VIPer100 ability to maintain its' power switch in the off state when the compensation voltage goes below 0.5V.

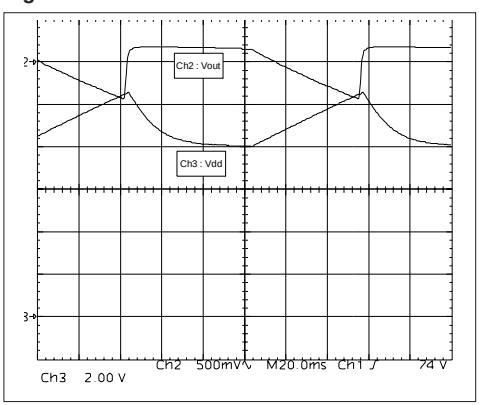
Figure 5. Good burst mode



This results in missing cycles, as shown on the following scope waveform (Vin = 400V, Iout = 30mA).

The burst mode has a recurring period of about 250µs, and 3 switching cycles take place each time. The output voltage ripple is about 1mV, and the Vdd voltage is stable, just above the low threshold voltage (8V) of the internal UVLO logic. This threshold can be reached by further reducing the output current, because it also reduces the Vdd voltage on the primary side (Less and less energy from the auxiliary winding). When this occurs, another type of burst mode appears, which is controlled by the Vdd voltage. This is called the “bad” burst mode, whereas the previous one is the “good” burst mode. The following scope waveform shows what happens in this case (Vin = 400V, Iout = 20mA).

Figure 6. Bad burst mode



Each time that the Vdd voltage reaches the low threshold voltage of the UVLO logic, the device is reset and the Vdd capacitor is charged back to the high threshold of this UVLO logic thanks to the start up current source which is turned on. The recurring period of this phenomenon is about 110ms. This behaviour leads to the following drawbacks :

1. Since the start up current source is activated to supply the device from the high voltage rail, the efficiency decreases dramatically.

2. The recurring period is very high, leading to a large output ripple. In the above example, this ripple is about 600mV, which is not acceptable for an output voltage of 5V.

3. This mode has very poor dynamic behaviour in the case of output current variation. If an increase of output current occurs during the recharging phase, the output capacitor will be discharged down to 0V and the normal output voltage will return only at the next starting phase.

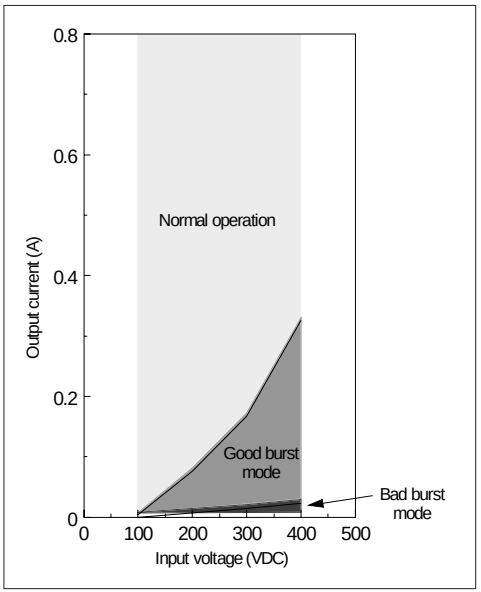
In conclusion, the good burst mode has to be extended in the low output power range as much as possible, mainly by optimizing the transformer. Paragraph 4.3 gives a good example of what can be achieved in this way.

The frontiers between the three modes of operation can be drawn on a curve according to the input voltage. Figure 7 shows this characteristics for the present design.

The bad burst mode occupies a very low range of output current, whereas the power supply doesn’t have its' nominal performance. But the output voltage is still under control (No overpassing of the nominal voltage), and no stress is applied to the power supply.

Note that figure 6 shows the worst case of bad burst mode, with an output current just below the limit of good burst mode. In this case, the output capacitor is deeply discharged, thus leading to the high ripple observed on this waveform. For lower current, this ripple becomes smaller, and is almost normal for very light load. See paragraph 3.3.1 for static load regulation performance.

Figure 7. Operation modes limits

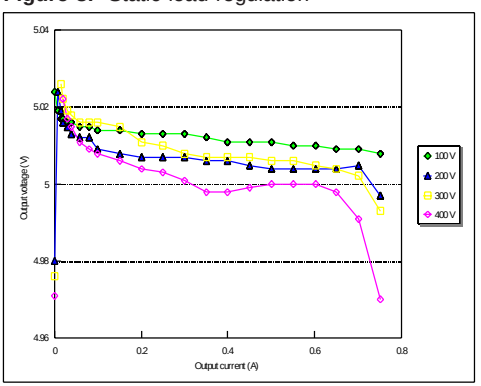


3.3. Load regulation

3.3.1. Static regulation

Figure 8 shows the output regulation for an output current ranging from 0A to 0.75A. Note that these measurements cover the three modes of operation (See paragraph 3.2).

Figure 8. Static load regulation



It can be seen that the bad burst mode leads to a slightly lower voltage than the nominal one, but is still convenient for voltage checking: If the power supply is operated without any load, the output voltage is still very close to the normal output voltage and this can be used for checking the output voltage. Also, the output ripple is far less than in figure 6, where the worst case was shown.

3.3.2. Dynamic regulation

The output current has been modulated by a square wave, from 50% to full load, and from 7% to full load, with an input voltage of 300VDC. The corresponding measurements are reported in figures 9 and 10.

Figure 10, where the output current varies from 50mA to 750mA, shows a case where the converter passes from good burst mode to normal operation (The limit between the two modes with this input voltage is about 170mA). It can be seen that this is completely transparent for the load, with a voltage transient of less than 100mVp for both transition polarities.

Figure 9. Dynamic behaviour for 50% to 100% of full load

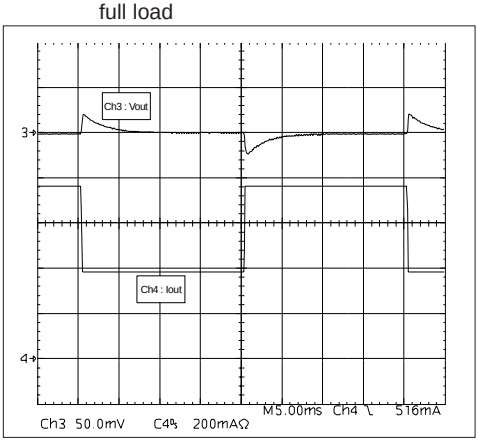
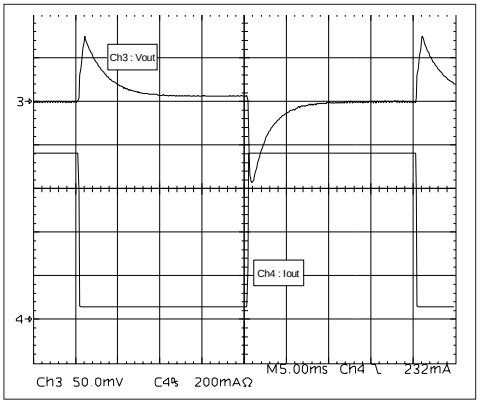


Figure 10. Dynamic behaviour for 7% to 100% of full load

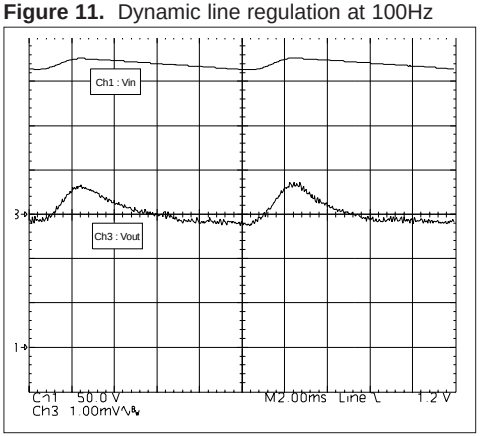


3.4. Line regulation

The power supply has been connected to standard 230VAC main lines, with a lower front capacitor for C1: Instead of a 100mF / 400V capacitor, a 10mF / 400V capacitor has been used in order to apply some voltage variation to the input of the power stage itself. Both the input voltage and output voltage are reported in figure 11, with a full load operation.

The 100Hz output ripple is less than 1mVpp, thanks to the excellent input voltage disturbances rejection of the device. The internal current control loop takes care of a good part of the input voltage variation, and the outer voltage loop is just making a final improvement, thus reducing the output voltage variation to such low levels.

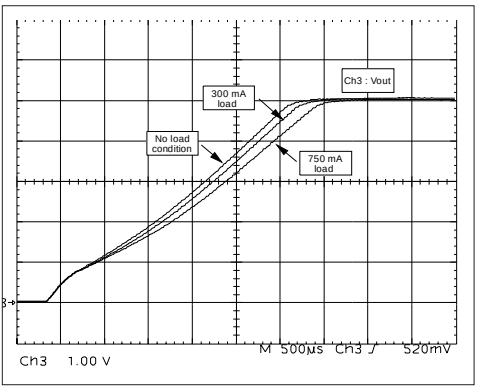
Figure 11. Dynamic line regulation at 100Hz



3.5.Turn on

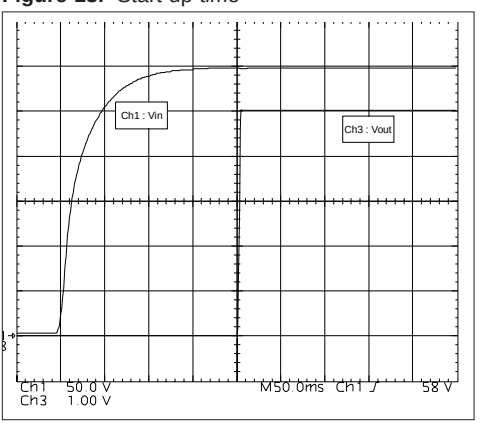
The input voltage of 300VDC has been suddenly applied to the power supply, and the output voltage monitored for three different load conditions. The results are reported in figure 12. It can be seen that the output voltage reaches its' final value in a monotone way, with no overshoot, and with a controlled slope. This slope is due to the high value of C5 which defines the soft start time of the power supply. This time can be easily adjusted by choosing the value of this capacitor. But the value of C3 must be changed accordingly, in order to maintain the Vdd voltage at a sufficient level during this soft start time.

Figure 12. Start up waveforms



The start up time has also been measured. This is given in figure 13, where both the input and output voltages are given at start up, for a full load condition. The start up time is about 200ms.

Figure 13. Start up time



3.6. Turn off

The behaviour of the power supply at turn off is reported in figures 14 and 15, for both the output and input voltages. It can be seen that the output voltage decreases in a monotone way, with no false restart after it reaches the zero level.

Figure 14. Turn off in no load condition

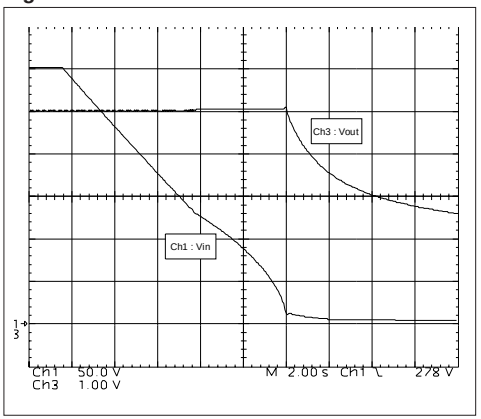
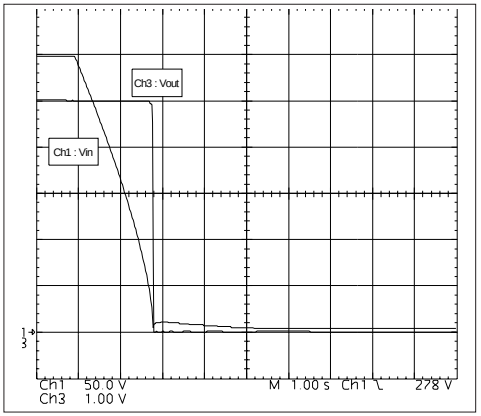


Figure 15. Turn off in full load condition



4. Improvements

Some modifications have been made on the design of figure 1, in order to study the impact of various parameters, or to improve the behaviour of the power supply. Here are the three items described in the following paragraphs :

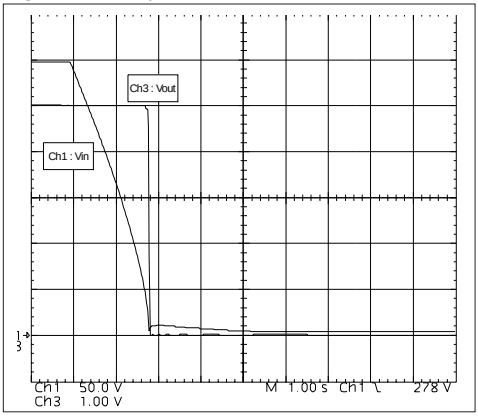
1. The short circuit condition has been experimented with, with an average output current of about 5A with the original schematics. It is clear that the transformer and the output diode are not able to withstand such an output current for a long time. Therefore, an improvement has been made in order to decrease the output current in case of short circuit. As a secondary consequence, this has a very good impact on the behaviour of the power supply, when operated in primary feedback configuration. Both topics are reported in paragraph 4.1.

2. Another transformer has been tried, with a power capability of 30W. Pretty good results are obtained, especially for the no load condition. The bad burst mode has been completely eliminated!

4.1. Short circuit conditions and primary regulation

With a 400VDC input voltage, a short circuit has been made on the output of the power supply. This results in a permanent average current of about 5A, well above what the transformer and the output diode are able to withstand. Figure 16 shows this short circuit current.

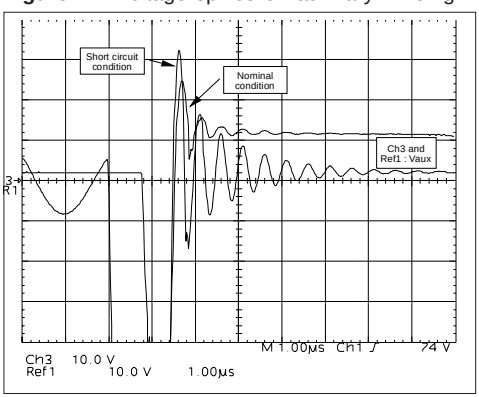
Figure 16. Output current in short circuit condition



The protection which is foreseen for the VIPer100 consists of a monitor of the Vdd voltage and to switch off the device when this voltage is below the low threshold voltage (8V) of the UVLO logic. This is done naturally when the output voltage is low (i.e. in short), because the auxiliary winding is delivering a Vdd voltage which is proportional to the output voltage.

Unfortunately, the used transformer is delivering some spikes of voltage at switch off on the auxiliary winding, as shown on figure 17. This is sufficient to send a correct supply to the device, and even to increase this voltage up to the internal reference one (13V) where the device decreases the peak current. Actually, the device is regulating its' primary Vdd voltage through the auxiliary winding spike. This explains the instabilities visible in figure 16, because nothing has been adapted to make this loop stable.

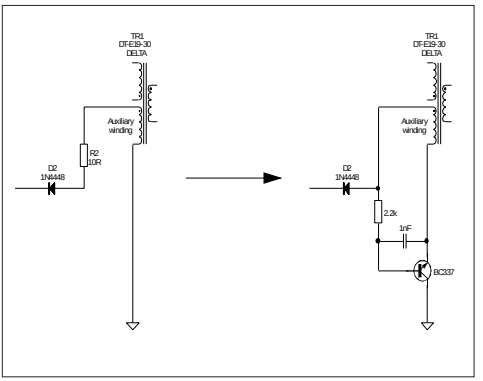
Figure 17. Voltage spikes on auxiliary winding



A solution to get rid of these spikes is to implement a filter, by just increasing R2. But this leads to poor performances in regulation, especially for light loads, where the bad burst mode will appear sooner (i.e. for larger current than in figure 7).
An another solution consists of using an active switch on the return line of the auxiliary winding. Figure 18 presents a possible schematic with only two more components, when compared with the former one.

A bipolar transistor is inserted in series with the auxiliary winding, and is driven through an R-C filter. This filter delays the turn on of the transistor when the auxiliary winding begins to deliver positive voltage, thus skipping the first spikes. Therefore, the Vdd voltage is more representative of what happens on the secondary side.

Figure 18. Possible short circuit protection

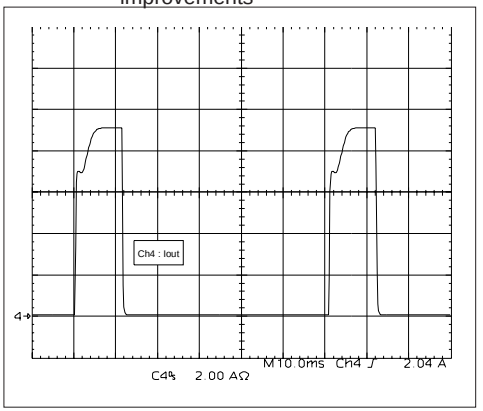


Note that R2 was doing the same thing, but in a less efficient manner. In nominal mode, this resistor avoids excessive Vdd voltage, which should reach the internal reference voltage and interferes with the secondary feedback. With the new design, it is possible to eliminate this resistor, and even to add two turns more on the auxiliary winding.

As a result, the short circuit current is no more limited by the Vdd voltage and it increases because the VIPer100 is internally limited to 4A, which is far too high when compared to the full load peak current. An external clamper must be added on the compensation pin to limit this current to more reasonable levels. A red LED has been used to limit this current at about 1A (1.5V on the compensation pin). Note that this clamper is not needed with a more suited product like VIPer20, which is internally limited to about 0.8A.

Figure 19 gives the output short circuit current with all these modifications (The one of figure 18 and a clamper on the compensation pin of the device), with an average output current of about 1.5A. This current is more acceptable than the previous one, and it appears that the converter is able to withstand indefinitely the short circuit condition. If a lower peak current is preferable (It reaches 9A on figure 19), it is still possible to adjust the peak current to lower values, because the nominal full load primary peak current is no more than 0.26A. The clamper could limit the compensation voltage to about 1V, corresponding to a maximum primary peak current of 0.5A.

Figure 19. Output short circuit current with improvements



Also note that an optimization of the transformer can lead to the same results. But the primary peak current must always be limited to a value compatible with the application. This could be done in most cases by the right device choice (VIPer100, VIPer50 or VIPer20).

This modification also provides good benefit when working with primary feedback: As the Vdd voltage is more representative of the secondary voltage, better regulation performances are obtained. Figure 20 compares the two static load regulations, with and without the modification. The following table gives the output voltage relative variation versus its' mean value for a load change from 10% to 100%.

Table 4.

	Relative Output Variation
Without Modification	+/- 12%
With Modification	+/- 3.8%

An improvement of more than three times can be observed. This allows us to consider the primary feedback as a serious possibility for simplifying low end power supplies, saving the cost of secondary feedback.

It can be seen on the previous graphic that the regulation with the modification is at its' worst at very low output current. This is due to the fact that less energy is passed to the Vdd capacitor for low duty cycles and/or burst mode. When in secondary feedback configuration, this means that the bad burst mode is appearing sooner, as shown in figure 21. But the usable range of the power supply still remains important, from about 6% to 100% of full load. The behaviour at 400VDC is even better.

Figure 20. Primary feedback static load regulation

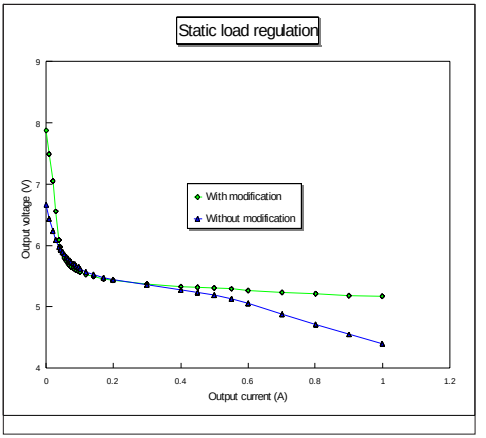
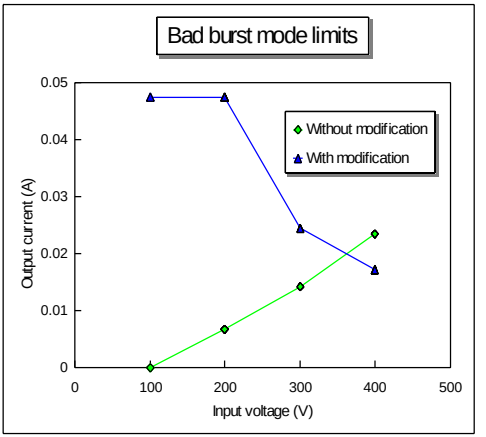


Figure 21. Bad burst mode limits with and without modification



4.2.Transformer modification

Another transformer has been tried. It has a larger volume than the previous one, and was designed to deliver an output voltage of 12V and a current of 2.5A. The other modifications are the following:

1. R7 has been omitted, and D5 has been replaced by a BZX55C10V. This zener voltage change allows the regulation at 12V. R2 has been replaced by a short.

2. D3 has been replaced by a BYW81P-200. Due to the higher output voltage, a schottky diode is no longer suitable. A standard one is used instead.

3. An LED in series with a resistor of 1.5kW has been added on the output. It indicates the correct operation of the power supply, and provides a bleeding load.

Only the efficiency has been measured. Results are shown in figure 26.

Figure 26. Efficiency

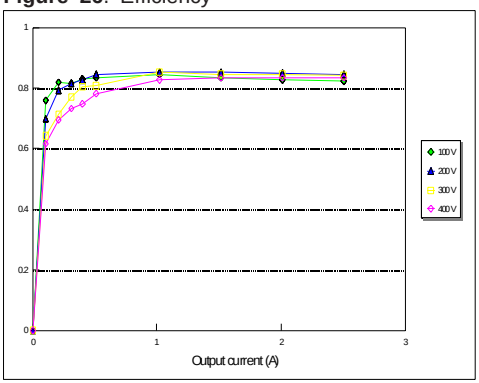
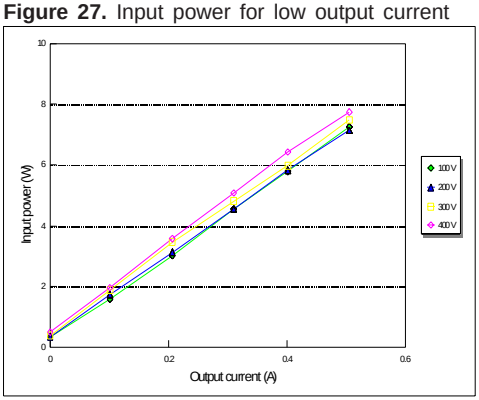


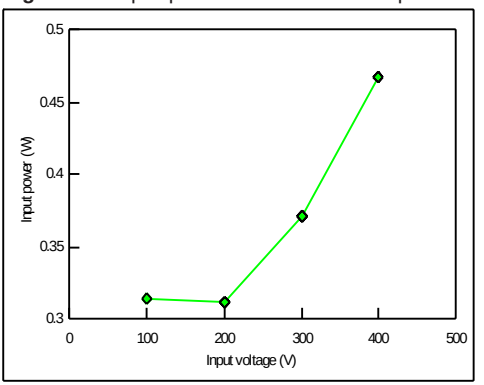
Figure 27. Input power for low output current



The efficiency is higher than 80% as soon as the output power exceeds 10W, and is typically 84% at full load (30W).

Also, it has been observed that no bad burst mode has taken place at low load, the whole range of power (0W to 30W) being covered in either good burst mode or normal operation, for all input voltages. The bleeding LED load is of course responsible of this behaviour, but it represents only 80mW of output power. As a results, the input power is becoming very low for low output load, as shown in figures 27 and 28. Note that although figure 28 is entitled “Input power for zero Watt output load”, it in fact represents the input power for an output power of 80mW due to the LED: In most cases, this power is absorbed by the standby load, where an LED is generally used.

Figure 28. Input power for zero Watt output load



5. Conclusion

It appears that the VIPer family is well suited for low level power supplies, such as the so called “standby” power supplies for which the full output power ranges from a few watts up to a few tens of watts. The most interesting points are:

1. The automatic burst mode which is implemented through an internal comparator on the compensation pin. This feature allows the control of very low load, by still maintaining a good efficiency, or offering very low input power for zero load operation. From this point of view, the design of the transformer is especially important, but the present note shows the good behaviour of the usual transformers.
2. In case the transformer doesn’t demonstrate a good behaviour in short circuit, a simple schematic (One low level bipolar transistor and one low voltage capacitor) greatly improves the protection of the whole power supply. At the same time, the primary feedback load regulation is improved by a factor of three.
3. The drain has been directly connected to the transformer, without any clamper or snubber. The avalanche capability of the device allows this cost saving, and experimentation has shown that this feature is only used at start up, the nominal operation peak primary voltage being lower than the breakdown voltage of the device.

The efficiency of the overall converter will be optimized by the choosing the right device, according to the required output power. For low output power levels, VIPer50 and VIPer20 are the most suitable.